Week 4-5 - Lesson 2.2 - Intro to NAND & NOR Logic

**Preface**

In the first lesson of this unit, we learned how to use a design process to transform design specifications into functional AOI combinational logic. Though the result of this work was a functioning circuit, this process does not address a few issues. First, Boolean algebra was required to simplify the logic expressions. Though Boolean algebra is an important mathematical process, applying its numerous theorems and laws is not always the easiest task to undertake. Second, as we will see in this lesson, AOI circuit implementations are rarely the most cost-effective solutions for combinational logic designs.

This lesson follows the standard APP (Activity/Project/Problem) format. After completing a series of guided foundational activities on Karnaugh Mappings, NAND only logic design, NOR only logic design, and MultSim’s Logic Converter, the students will apply the *Combinational Logic Design Process* (version 2) to develop a *Fireplace Control Circuit*. This process will walk the students through the steps required to transform a set of written design specifications into a functional combinational logic circuit implemented with either NAND only or NOR only logic.

**Concepts**

1.      Karnaugh Mapping is a graphical technique for simplifying logic expressions containing two, three, and four variables.

2.      A don’t care condition is a situations where the design specifications “don’t care” what the output is for one or more input conditions. Don’t care conditions in K-Maps can lead to significantly simpler logic expressions and circuit implementations.

3.      A NAND gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an inverter gate. Any combinational logic expression can be implemented using only NAND gates.

4.      A NOR gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an inverter gate. Any combinational logic expression can be implemented using only NOR gates.

5.      There is a formal design process for translating a set of design specifications into a functional combinational logic circuit implement with NAND or NOR gates.

6.      Combinational logic designs implemented with NAND gates or NOR gates will typically required fewer Integrated Circuits (IC) than AOI equivalent implementations.

**Standards and Benchmarks Addressed**

***Standards for Technological Literacy***

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| **Standard 1:  Students will develop an understanding of the characteristics and scope of technology.** | |
| **BM J:** | The nature and development of technological knowledge and processes are functions of the setting. |
| **BM L:** | Inventions and innovations are the results of specific, goal-directed research. |
| **BM M:** | Most development of technologies these days is driven by the profit motive and the market. |
| **Standard 2:  Students will develop an understanding of the core concepts of technology.** | |
| **BM W:** | Systems’ thinking applies logic and creativity with appropriate compromises in complex real-life problems. |
| **BM X:** | Systems, which are the building blocks of technology, are embedded within larger technological, social, and environmental systems. |
| **BM Y:** | The stability of a technological system is influenced by all of the components in the system especially those in the feedback loop. |
| **BM Z:** | Selecting resources involves trade-offs between competing values, such as availability, cost, desirability, and waste. |
| **BM AA:** | Requirements involve the identification of the criteria and constraints of a product or system and the determination of how they affect the final design and development. |
| **BM BB:** | Optimization is an on going process or methodology of designing or making a product and is dependent on criteria and constraints. |
| **BM CC:** | New technologies create new processes. |
| **BM DD:** | Quality control is a planned process to ensure that a product, service, or system meets established criteria. |
| **BM FF:** | Complex systems have many layers of controls and feedback loops to provide information. |
| **Standard 3:  Students will develop an understanding of the relationships among technologies and the connections between technology and other fields of study.** | |
| **BM G:** | Technology transfer occurs when a new user applies an existing innovation developed for one purpose in a different function |
| **BM H:** | Technological innovation often results when ideas, knowledge, or skills are shared within a technology, among technologies, or across other fields. |
| **BM J:** | Technological progress promotes the advancement of science and mathematics. Likewise, progress in science and mathematics leads to advances in technology. |
| **Standard 9:  Students will develop an understanding of engineering design.** | |
| **BM I:** | Established design principles are used to evaluate existing designs, to collect data, and to guide the design process. |
| **BM J:** | Engineering design is influenced by personal characteristics, such as creativity, resourcefulness, and the ability to visualize and think abstractly. |
| **BM K:** | A prototype is a working model used to test a design concept by making actual observations and necessary adjustments. |
| **BM L:** | The process of engineering design takes into account a number of factors. |
| **Standard 10:  Students will develop an understanding of the role of troubleshooting, research and development, invention and innovation, and experimentation in problem solving.** | |
| **BM I:** | Research and development is a specific problem-solving approach that is used intensively in business and industry to prepare devices and systems for the marketplace. |
| **BM J:** | Technological problems must be researched before they can be solved. |
| **BM K:** | Not all problems are technological, and not every problem can be solved using technology. |
| **BM L:** | Many technological problems require a multidisciplinary approach. |
| **Standard 11:  Students will develop abilities to apply the design process.** | |
| **BM M:** | Identify the design problem to solve and decide whether or not to address it. |
| **BM N:** | Identify criteria and constraints and determine how these will affect the design process. |
| **BM O:** | Refine a design by using prototypes and modeling to ensure quality, efficiency, and productivity of the final product. |
| **BM P:** | Evaluate the design solution using conceptual, physical, and mathematical models at various intervals of the design process in order to check for proper design and to note areas where improvements are needed. |
| **BM Q:** | Develop and produce a product or system using a design process. |
| **BM R:** | Evaluate final solutions and communicate observation, processes, and results of the entire design process, using verbal, graphic, quantitative, virtual, and written means, in addition to three-dimensional models. |
| **Standard 12:  Students will develop the abilities to use and maintain technological products and systems.** | |
| **BM L:** | Document processes and procedures and communicate them to different audiences using appropriate oral and written techniques. |
| **BM M:** | Diagnose a system that is malfunctioning and use tools, materials, machines, and knowledge to repair it. |
| **BM N:** | Troubleshoot, analyze, and maintain systems to ensure safe and proper function and precision. |
| **BM O:** | Operate systems so that they function in the way they were designed. |
| **BM P:** | Use computers and calculators to access, retrieve, organize and process, maintain, interpret, and evaluate data and information in order to communicate. |
| **Standard 13:  Students will develop the abilities to assess the impacts of products and systems.** | |
| **BM J:** | Collect information and evaluate its quality. |
| **Standard 17:  Students will develop an understanding of and be able to select and use information and communication technologies.** | |
| **BM L:** | Information and communication technologies include the inputs, processes, and outputs associated with sending and receiving information. |
| **BM M:** | Information and communication systems allow information to be transferred from human to human, human to machine, machine to human, and machine to machine. |
| **BM N:** | Information and communication systems can be used to inform, persuade, entertain, control, manage, and educate. |
| **BM O:** | Communication systems are made up of source, encoder, transmitter, receiver, decoder, storage, retrieval, and destination. |
| **BM P:** | There are many ways to communicate information, such as graphic and electronic means. |
| **BM Q:** | Technological knowledge and processes are communicated using symbols, measurement, conventions, icons, graphic images, and languages that incorporate a variety of visual, auditory, and tactile stimuli. |

***National Science Education Standards***

**Standard K-12: Unifying Concepts and Processes:**  As a result of activities in grades K-12, all students should develop understanding and abilities aligned with the following concepts and processes;

         Systems, order, and organization

         Evidence, models, and explanation

         Form and function

**Standard A: Science As Inquiry:** As a result of activities in grades 9-12, all students should develop;

         Abilities necessary to do scientific inquiry

         Understandings about scientific inquiry

**Standard E: Science and Technology:** As a result of activities in grades 9-12, all students should develop

         Abilities of technological design

***Principles and Standards for School Mathematics***

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| **Number and Operations:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; understand numbers, ways of representing numbers, relationships among numbers, and number systems; understand meanings of operations and how they relate to one another; compute fluently and make reasonable estimates. |
| **Algebra:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; understand patterns, relations, and functions; represent and analyze mathematical situations and structures using algebraic symbols;  use mathematical models to represent and understand quantitative relationships; analyze change in various contexts. |
| **Measurement:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; understand measurable attributes of objects and the units, systems, and processes of measurement; apply appropriate techniques, tools, and formulas to determine measurements. |
| **Data Analysis and Probability:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; formulate questions that can be addressed with data and collect, organize, and display relevant data to answer them; select and use appropriate statistical methods to analyze data; develop and evaluate inferences and predictions that are based on data; understand and apply basic concepts of probability. |
| **Problem Solving:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; build new mathematical knowledge through problem solving; solve problems that arise in mathematics and in other contexts; apply and adapt a variety of appropriate strategies to solve problems; monitor and reflect on the process of mathematical problem solving. |
| **Reasoning and Proof:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; recognize reasoning and proof as fundamental aspects of mathematics; make and investigate mathematical conjectures; develop and evaluate mathematical arguments and proofs; select and use various types of reasoning and methods of proof. |
| **Communication:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; organize and consolidate their mathematical thinking through communication; communicate their mathematical thinking coherently and clearly to peers, teachers, and others; analyze and evaluate the mathematical thinking and strategies of others; use the language of mathematics to express mathematical ideas precisely. |
| **Connections:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; recognize and use connections among mathematical ideas; understand how mathematical ideas interconnect and build on one another to produce a coherent whole; recognize and apply mathematics in contexts outside of mathematics. |
| **Representation:** | Instructional programs from pre-kindergarten through grade 12 should enable all students to; create and use representations to organize, record, and communicate mathematical ideas; select, apply, and translate among mathematical representations to solve problems; use representations to model and interpret physical, social, and mathematical phenomena. |

***Standards for English Language Arts***

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| **Standard 4:** | Students adjust their use of spoken, written, and visual language (e.g. conventions, style, vocabulary) to communicate effectively with a variety of audiences and for different purposes. |
| **Standard 12:** | Students use spoken, written and visual language to accomplish their own purposes (e.g. for learning, enjoyment, persuasion, and the exchange of information). |

**Performance Objectives**

*It is expected that students will:*

         Use the K-Mapping technique to simplify combinational logic problems containing two, three, and four variables.

         Be able to solve K-Maps that contain one or more *don’t care* conditions.

         Design combinational logic circuit using NAND and NOR logic gates.

         Translate a set of design specifications into a functional NAND or NOR combinational logic circuit following a formal design process.

         Be able to compare and contrast the quality of combinational logic designs implemented with AOI, NAND, and NOR logic gates.

         Use Circuit Design Software (CDS) and a Digital Logic Board (DLB) to simulate and prototype NAND and NOR logic circuits.

**Assessment**

*Explanation*

         Students will explain the differences between NAND andNOR logic.

*Application*

         Students will demonstrate to an adminstrator how to K-Map a combinational logic problem

*Self-knowledge*

         Students will create a brainstorming list of improvements that could be made to the CDS software and justify why these changes would make the learning curve easier for students.

**Essential Questions**

1.      What is the process for using the K-Mapping technique to simplify a logic expression? What are the advantages of using this process over Boolean algebra?

2.      What is a *don’t care* condition, and how can it be used in a K-Map to reduce the complexity of the combinational logic design?

3.      What does the term universal gate mean? Why are NAND gates and NOR gates considered universal gates?

4.      What is the advantage of implementing a combinational logic design with only NAND gates (or NOR gates)?

5.      What are the steps in the design process for converting an AOI combinational logic design into a NAND only or NOR only design?

6.      Typically, what is the advantage of NAND only design (or NOR only design) over an AOI design? Why is it important to it compare both the NAND only and NOR only designs?

**Key Terms**

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| **Adjacent Cell** | Two cells in a K-map are adjacent if there is only one variable that is different between the coordinates of the two cells. |
| **Cell** | The smallest unit of Karnaugh map, corresponding to one line of a truth table. The input variables are the cell’s coordinates and the output variable is the cell’s contents. |
| **Don’t Care Condition** | Situation when a circuit’s output level for a given set of input conditions can be assigned as either a 1 or 0. |
| **Karnaugh Map** | A graphical tool for finding the maximum SOP or POS simplification of a Boolean expression. A Karnaugh map works by arranging the terms of an expression so that variable scans are cancelled by grouping minterms or maxterms. |
| **NAND Gate** | Logic circuit that operates like an AND gate followed by an INVERTER. The output of a NAND gate is LOW (logic level 0) only if all inputs are HIGH (logic level 1). |
| **NOR Gate** | Logic circuit that operates like an OR gate followed by an INVERTER. The output of a NOR gate is LOW (logic level 0) when any or all inputs are HIGH (logic level 1). |

**Day-by-Day Plans**

*Time: 14 days*

**Day 1 – 2: Lesson Overview and Karnaugh Mapping**

         The teacher will present [**Concepts**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/L2_2NANDNORLogic.htm#concepts), [**Essential Questions**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/L2_2NANDNORLogic.htm#questions), and [**Key Terms**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/L2_2NANDNORLogic.htm#terms) in order to provide a lesson overview.

         The teacher will present [**Karnaugh Mapping.ppt.**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/KMapping.ppt)

         Students will take notes in their engineering journals.

         The teacher will distribute and introduce [**Activity 2.2.1 K-Mapping**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_1KMapping.htm).

         Students will work on Activity 2.2.1 K-Mapping.

**Day 3 – 5: NAND Logic Implementation**

         The teacher will present [**Universal Gate – NAND.ppt.**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/UniversalNAND.ppt)

         Students will take notes in their engineering journals.

         The teacher will distribute and introduce [**Activity 2.2.2 NAND Logic Design**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_2NANDLogicDesign.htm).

         Students will work on Activity 2.2.2 NAND Logic Design.

**Day 6 – 8: NOR Logic Implementation**

         The teacher will present [**Universal Gate – NOR.ppt.**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/UniversalNOR.ppt)

         Students will take notes in their engineering journals.

         The teacher will distribute and introduce [**Activity 2.2.3 NOR Logic Design**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_3NORLogicDesign.htm).

         Students will work on Activity 2.2.3 NOR Logic Design.

**Day 9: Logic Converter**

         The teacher will give a brief demonstration on the MultiSim Logic Converter.

         Students will take notes in their engineering journals.

         The teacher will distribute and introduce [**Activity 2.2.4 Logic Converter**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_4LogicConverter.htm).

         Students will work on Activity 2.2.4 Logic Converter.

**Day 10 – 13 Fireplace Control Circuit Design, Simulation and Prototyping**

         The teacher will present [**Comb Logic Design Process (v2).ppt.**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/ComboLogicDesignProcess.ppt)

         The teacher will distribute and introduce [**Project 2.2.5 Fireplace Control Circuit.**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/P2_2_5FireplaceControlCircuit.htm)

         Students will take notes in their engineering journals.

         Students will work on Project 2.2.5 Fireplace Control Circuit.

         The teacher will assist the students as needed.

**Instructional Resources**

Presentations

[**Karnaugh Mapping**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/KMapping.ppt)

[**Universal Gate – NAND**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/UniversalNAND.ppt)

[**Universal Gate - NOR**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/UniversalNOR.ppt)

[**Comb Logic Design Process**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Powerpoints/ComboLogicDesignProcess.ppt)

Word Documents

[**Lesson 2.2 Key Term Crossword**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/L2_2KeyTermCrossword.doc)

[**Activity 2.2.1 K-Mapping**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_1KMapping.doc)

[**Activity 2.2.2 NAND Logic Design**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_2NANDLogicDesign.doc)

[**Activity 2.2.3 NOR Logic Design**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_3NORLogicDesign.doc)

[**Activity 2.2.4 Logic Converter**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/A2_2_4LogicConverter.doc)

[**Project 2.2.5 Fireplace Control Circuit**](mk:@MSITStore:C:\Documents%20and%20Settings\DAVID_ROEMER\Desktop\DE\DE_2009.chm::/Unit_2/Activities/P2_2_5FireplaceControlCircuit.doc)